



# United States Patent and Trademark Office

UNITED STATES DEPARTMENT OF COMMERCE United States Patent and Trademark Office Address: COMMISSIONER OF PATENTS AND TRADEMARKS P.O. Box 1450 Alexandria, Virginia 22313-1450 www.capio.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.		
10/053,300	01/17/2002	Vishnu K. Agarwal	303.780US1	5007		
	590 05/08/2003					
SCHWEGMAN, LUNDBERG, WOESSNER & KLUTH, P.A. P.O. BOX 2938			EXAMINER			
MINNEAPOLI			PHAM, HOAI V			
			ART UNIT	PAPER NUMBER		
			2814			
	·			DATE MAILED: 05/08/2003		

Please find below and/or attached an Office communication concerning this application or proceeding.

<u> </u>		Application No.		-
`			Applicant(s)	
Office Action Summary		10/053,300	AGARWAL ET AL	••
		Examiner	Art Unit	
	The MAILING DATE of this communication or Reply	Hoai V Pham	2814	
Period f	• •			dress
- External control con	MAILING DATE OF THIS COMMUNICATION OF THIS C	JN. R 1.136(a). In no event, however, m . reply within the statutory minimum riod will apply and will expire SIX (6)	nay a reply be timely filed  of thirty (30) days will be considered timely MONTHS from the mailing date of this continuous	, mmunication.
1)[	Responsive to communication(s) filed on	24 March 2003		
2a)□		This action is non-final.		
3)	/23			
Dispositi	Since this application is in condition for all closed in accordance with the practice uncon of Claims	ler Ex parte Quayle, 1935	matters, prosecution as to the C.D. 11, 453 O.G. 213.	e merits is
4)🖂	Claim(s) 1-28 and 58-77 is/are pending in	he application.		
	4a) Of the above claim(s) is/are witho			
5)	Claim(s) is/are allowed.			
6)⊠	Claim(s) <u>1-28 and 58-77</u> is/are rejected.			
7)	Claim(s) is/are objected to.			
8)	Claim(s) are subject to restriction and	d/or election requirement.		
Application	on Papers			
	he specification is objected to by the Exami			-
10)⊠ T	he drawing(s) filed on is/are: a)∏ ac	cepted or b) abjected to b	y the Examiner.	
44) 🗔 🖚	Applicant may not request that any objection to	the drawing(s) be held in ab	eyance. See 37 CFR 1.85(a).	
11)[_][]	ne proposed drawing correction filed on	is: a)[] approved b)[	disapproved by the Examiner.	
	ir approved, corrected drawings are required in	reply to this Office action.		
	ne oath or declaration is objected to by the I	Examiner.		
	der 35 U.S.C. §§ 119 and 120			
13) A	cknowledgment is made of a claim for forei	gn priority under 35 U.S.C	C. § 119(a)-(d) or (f).	
a)[_	All b) Some * c) None of:			
1	Certified copies of the priority document	nts have been received.		
2	Certified copies of the priority documer	nts have been received in	Application No.	
3.	Copies of the certified copies of the pri application from the International B the attached detailed Office action for a lis	ority documents have bee	en received in this National Sta	age
14)∐ Ack	nowledgment is made of a claim for domes	tic priority under 35 H S C	S 110(a) (to a province of	
a)	☐ The translation of the foreign language precond to the foreign language preconding to the foreign language.  ■ The foreign language preconding the foreign language preconding to the foreign language preconding the foreign language preconding the foreign language preconding to the foreign language preconding the foreign language precondin	ovisional application has	heen received	plication).
Notice of Notice of Notice of Notice of Information	f References Cited (PTO-892) f Draftsperson's Patent Drawing Review (PTO-948) on Disclosure Statement(s) (PTO-1449) Paper No(s)	E\	v Summary (PTO-413) Paper No(s). f Informal Patent Application (PTO-15	
Patent and Trader O-326 (Rev. 0	4.04)	ction Summary		

### **DETAILED ACTION**

### Election/Restrictions

1. Applicant's election without traverse of claims 1-28 and 58-77 in Paper No. 3 is acknowledged.

#### **Drawings**

- 2. The drawings are objected to under 37 CFR 1.83(a). The drawings must show every feature of the invention specified in the claims. Therefore, the transistor must be shown or the feature(s) canceled from the claim(s). No new matter should be entered.
- A proposed drawing correction or corrected drawings are required in reply to the Office action to avoid abandonment of the application. The objection to the drawings will not be held in abeyance.

## Claim Rejections - 35 USC § 112

- 4. The following is a quotation of the second paragraph of 35 U.S.C. 112:
  The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.
- 5. Claims 16 and 17-28, 58-77 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

Claim 16, "a third layer about the process stack" renders the claim indefinite. It is not clear how "a third layer about the process stack" define the claim structure.

Art Unit: 2814

What does "a third layer about the process stack" mean? Where is "a third layer about the process stack" located?

Claims 17 and 24, line 5, "a process stack extending away from the surface" renders the claim indefinite. It is not clear how "a process stack" extending away from the surface of the substrate.

Claim 28, 58, 64, 72, and 75, "a transistor on the substrate, the transistor being formed from a process stack having" renders the claim indefinite because:

- > It is not clear how the transistor can be formed by a process stack while the specification pages 6-9 shows that the process stack is used to form the trench isolation.
- > The oxide layer and the nitride layer have been removed before forming the transistor thus there is no oxide and nitride layers left in the final structure (see fig. 6B, pages 9-10).

## Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that 6. form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless -

- (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.
- 7. Claims 1-3, 5-7, 9, 12-15, 28 are rejected under 35 U.S.C. 102(b) as being anticipated by Furukawa et al. [U.S. Pat. 5,798,553].

Art Unit: 2814

With respect to claims 1, 6, 9, and 15, Furukawa et al. (figs. 2A-2G, cols. 3-7) discloses an apparatus, comprising:

a substrate (10) having at least one trench wall (26A, 26B);

a first layer (14);

a second layer (14) (see col. 4, lines 1-3) wherein the first layer, the second layer and a portion of the substrate form a process stack, the first and second layers being a pull back distance from the trench wall thereby forming an implant region having a migration region; and

a dopant in the implant region and migration regions (see fig. 2G).

Furukawa et al. discloses the same structure of applicant invention. Therefore, those skilled in the art would recognize that a central area underneath the first layer having a threshold voltage that is about substantially uniform.

With respect to claim 2, Furukawa et al. discloses that the pull back distance is in a range from about 25 A to about 300 A (see fig. 2F, col. 6, lines 14-15).

With respect to claim 3, Furukawa et al. discloses that the pull back distance is substantially symmetrical about the second layer.

With respect to claims 5 and 13, Furukawa et al. discloses that the dopant has an implant energy in a preferred implant energy range from about 5 to about 25 keV (see col. 7, lines 10-15).

With respect to claim 7, Furukawa et al. discloses the same structure of applicant invention. Therefore, those skilled in the art would recognize that the dopant in the implant region changes an electrical characteristic of the implant region thereby making

Art Unit: 2814

a threshold voltage in the implant region about equivalent to or greater than a threshold voltage in the central area of the substrate underneath the first layer.

With respect to claim 12, Furukawa et al. discloses that the dopant is one of Boron (see col. 7, lines 10-14).

With respect to claim 14, Furukawa et al. discloses that the implant energy is in a more preferred implant energy range of less than or equal to about 10 keV (see col. 7, lines 10-15).

8. Claims 1, 3, 6-7, 9, 10, 15, 17, 19, and 22-23 are rejected under 35 U.S.C. 102(b) as being anticipated by Oh et al. [U.S. Pat. H204].

With respect to claims 1, 6, 9, 15, and 17, Oh et al. (figs. 2-10, cols. 2-5) discloses an apparatus, comprising:

a substrate (30) having at least one trench wall (54, 56) (see fig. 7);

a first layer (32, oxide);

a second layer (34, nitride) wherein the first layer, the second layer and a portion of the substrate form a process stack, the first and second layers being a pull back distance from the trench wall thereby forming an implant region (62, 64); and

a dopant in the implant region (see fig. 7).

Oh et al. discloses the same structure of applicant invention. Therefore, those skilled in the art would recognize that a central area underneath the first layer having a threshold voltage that is about substantially uniform.

Application/Control Number: 10/053,300 Page 6

Art Unit: 2814

With respect to claim 3, Oh et al. discloses that the pull back distance is substantially symmetrical about the second layer (see fig. 7).

With respect to claim 7, Oh et al. discloses the same structure of applicant invention. Therefore, those skilled in the art would recognize that the dopant in the implant region changes an electrical characteristic of the implant region thereby making a threshold voltage in the implant region about equivalent to or greater than a threshold voltage in the central area of the substrate underneath the first layer.

With respect to claim 10, Oh et al. discloses that the substrate is a P-type substrate and the dopant is a P-type dopant (see col. 2, line 46 and col. 3, lines 43-46).

With respect to claim 12, Oh et al. discloses that the dopant is one of Boron (see col. 3, lines 43-46).

With respect to claim 19, Oh et al. discloses that the dopant (62, 64) is present in the substrate at the at least one trench wall (see fig. 7).

With respect to claims 22-23, Oh et al. discloses that the implant region occupies a migration region adjacent to the oxide layer (see fig. 7).

### Claim Rejections - 35 USC § 103

9. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

- 10. This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).
- 11. Claim 4 is rejected under 35 U.S.C. 103(a) as being unpatentable over Furukawa et al. [U.S. Pat. 5,798,553].

Furukawa et al. does not teach the exact concentration, as claimed by Applicant. However, the concentration range would have been obvious to an ordinary artisan practicing the invention because, absent evidence of disclosure of criticality for the range giving unexpected results, it is not inventive to discover optimal or workable ranges by routine experimentation. *In re Aller*, 220 F.2d 454, 105 USPQ 233, 235 (CCPA 1955).

12. Claim 8 is rejected under 35 U.S.C. 103(a) as being unpatentable over Furukawa et al. [U.S. Pat. 5,798,553] as applied to claims 6-7 above, and further in view of Parekh et al. [U.S. Pat. 5,945,724].

Furukawa et al. discloses all the limitation as claimed above except: the substrate further includes a corner region having a rounded contour. However, Parekh et al. discloses that the substrate includes a corner region (31a, 31b) having a rounded

contour (see fig. 3, col. 7, lines 1-19). Therefore, it would have been obvious to one having skill in the art at the time the invention was made to have the substrate having a rounded corner as taught by Parekh et al. into the device of Furukawa et al. in order to prevent leakage current and to provide better filling material in the trench while reducing the critical dimension for the trench width.

13. Claims 2, 4, 5, 11, 13, 14, and 18, are rejected under 35 U.S.C. 103(a) as being unpatentable over Oh et al. [U.S. Pat. H204].

With respect to claims 2, 4, 5, 13, 14, and 18, Oh et al. does not teach the exact pull back distance, a concentration, an implant energy, as claimed by Applicant.

However, the pull back distance, the concentration, the implant energy range would have been obvious to an ordinary artisan practicing the invention because, absent evidence of disclosure of criticality for the range giving unexpected results, it is not inventive to discover optimal or workable ranges by routine experimentation. *In re Aller*, 220 F.2d 454, 105 USPQ 233, 235 (CCPA 1955).

With respect to claim 11, Oh et al. does not disclose an N-type substrate and an N-type dopant. However, It will be apparent to those skilled in the art that the opposite conductivity types can be substituted for the substrate and the dopant.

14. Claims 8, 20, and 21 are rejected under 35 U.S.C. 103(a) as being unpatentable over Oh et al. [U.S. Pat. H204] as applied to claims 6-7 above, and further in view of Parekh et al. [U.S. Pat. 5,945,724].

Art Unit: 2814

Oh et al. discloses all the limitation as claimed above except: the at least one trench wall is angled in relation to the surface and the substrate includes a corner region having a rounded contour. However, Parekh et al. discloses that the at least one trench wall is angled in relation to the surface and the substrate includes a corner region (31a, 31b) having a rounded contour (see fig. 3, col. 6, lines 16-30 and col. 7, lines 1-19). Therefore, it would have been obvious to one having skill in the art at the time the invention was made to have the at least one trench wall is angled in relation to the surface and the substrate includes a corner region (31a, 31b) having a rounded contour, as taught by Parekh et al., into the device of Oh et al. in order to prevent leakage current and to provide better filling material in the trench while reducing the critical dimension for the trench width.

Page 9

15. Claims 24-27, as best understood, are rejected under 35 U.S.C. 103(a) as being unpatentable over Furukawa et al. [U.S. Pat. 5,798,553] in view of Oh et al. [U.S. Pat. H204].

With respect to claims 24 and 27, Furukawa et al. (figs. 2A-2G, cols. 3-7) discloses an apparatus having reduced transistor leakage attributes, comprising:

a substrate (10) having a surface, a comer region and at least one trench wall (26A, 26B) (see fig. 2E);

a stack layer (14) and a portion of the substrate form a process stack formed on the surface, the stack layer (14) being a pull back distance in a range from about 25 A to about 300 A from the trench wall thereby forming an implant region, the pull back

distance being substantially symmetrical about the stack layer (14), the comer region of the substrate comprising a part of the implant region; and

a dopant in the implant region thereby changing an electrical characteristic of the implant region and making a threshold voltage in the comer region about equivalent to or greater than a threshold voltage in a central area of the substrate underneath the oxide layer, the threshold voltage of the central area of the substrate being about substantially uniform.

Furukawa et al. discloses that the stack layer (14) can be used various other layer or combinations of layers (see col. 4, lines 51-55). Furukawa et al. does not disclose that the stack layer (14) comprises an oxide layer and a nitride layer on the oxide layer. However, Oh et al. discloses that an oxide layer (32) and a nitride layer (34) on the oxide layer and their uses are well known in the art for forming the stack layer (see fig. 2, col. 3, lines 23-28). Therefore, it would have been obvious to one having skill in the art at the time the invention was made to select oxide and nitride as known materials, as taught by Oh et al. into the device of Furukawa et al. in order to use as a mask for etching the trench in the substrate. Moreover, selection of a known material based on its suitability for its intended use supported a prima facie obviousness determination in Sinclair & Carroll Co., Inc. v. Interchemical Corp., 325 U.S. 327, 65 USPQ 297 (1945).

With respect to claim 25, Furukawa et al. discloses that the dopant is one of Boron (see col. 7, lines 10-15).

Claim 27 is rejected under 35 U.S.C. 103(a) as being unpatentable over 16. Furukawa et al. [U.S. Pat. 5,798,553] and Oh et al. [U.S. Pat. H204] as applied to claims 24-25 above, and further in view of Parekh et al. [U.S. Pat. 5,945,724].

Furukawa et al. and Oh et al. disclose all the limitation as claimed above except: the corner region having a rounded contour. However, Parekh et al. discloses that the corner region (31a, 31b) having a rounded contour (see fig. 3, col. 7, lines 1-19). Therefore, it would have been obvious to one having skill in the art at the time the invention was made to have the rounded corner as taught by Parekh et al. into the device of Furukawa et al. in order to prevent leakage current and to provide better filling material in the trench while reducing the critical dimension for the trench width.

17. Claim 28, as best understood, is rejected under 35 U.S.C. 103(a) as being unpatentable over Furukawa et al. [U.S. Pat. 5,798,553] in view of Parekh et al. [U.S. Pat. 5,945,724].

Furukawa et al. (figs. 2A-2G, cols. 3-7) discloses a transistor structure having reduced transistor leakage attributes, comprising:

a substrate (10) having a surface, a corner region and at least one trench wall (26A, 26B);

- a dopant in the corner region (fig. 2G);
- a third layer forming a plug in a shallow trench isolation of the substrate; and a transistor on the substrate (col. 7, lines 43-47).

Furukawa et al. fails to disclose the corner region having a rounded contour. However, Parekh et al. discloses that the corner region (31a, 31b) having a rounded contour (see fig. 3, col. 7, lines 1-19). Therefore, it would have been obvious to one having skill in the art at the time the invention was made to have the substrate having a rounded corner as taught by Parekh et al. into the device of Furukawa et al. in order to prevent leakage current and to provide better filling material in the trench while reducing the critical dimension for the trench width.

18. Claim 58-62, 64-76, as best understood, are rejected under 35 U.S.C. 103(a) as being unpatentable over Furukawa et al. [U.S. Pat. 5,798,553] in view of Salling et al. [U.S. Pat. 6,515,889].

Furukawa et al. (figs. 2A-2G, cols. 3-7) discloses a shallow trench isolation having reduced transistor leakage attributes, comprising:

- a substrate (10) having a surface, a corner region and at least one trench wall (26A, 26B);
  - a dopant in the corner region (fig. 2G);
- a central area underneath the transistor having a threshold voltage that is about substantially uniform (fig. 2G);
  - a third layer forming a plug in the shallow trench isolation of the substrate; and a transistor on the substrate (col. 7, lines 43-47).

Furukawa et al. does not disclose that the shallow trench isolation is used in an electronic system. However, Salling et al. discloses that the shallow trench isolation

(105) is used in the electronic system (fig. 10, col. 11, lines 56-61). Therefore, it would have been obvious to one having skilled in the art at the time the invention was made to use the shallow trench isolation in the electronic system as taught by Salling et al. in order to prevent leakage current entering the active device.

19. Claims 63 and 77 are rejected under 35 U.S.C. 103(a) as being unpatentable over Furukawa et al. [U.S. Pat. 5,798,553] and Salling et al. [U.S. Pat. 6,515,889] as applied to claims 58-62, 64-76 above, and further in view of Parekh et al. [U.S. Pat. 5,945,724].

Furukawa et al. discloses all the limitation as claimed above except: the corner region having a rounded contour. However, Parekh et al. discloses that the corner region (31a, 31b) having a rounded contour (see fig. 3, col. 7, lines 1-19). Therefore, it would have been obvious to one having skill in the art at the time the invention was made to have the substrate having a rounded corner as taught by Parekh et al. into the device of Furukawa et al. in order to prevent leakage current and to provide better filling material in the trench while reducing the critical dimension for the trench width.

### Conclusion

20. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Hoai V Pham whose telephone number is 703-308-6173. The examiner can normally be reached on 6:30A.M. - 6:00P.M..

Art Unit: 2814

Page 14

- 21. If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Wael M. Fahmy can be reached on 703-308-4918. The fax phone numbers for the organization where this application or proceeding is assigned are 703-308-7722 for regular communications and 703-308-7724 for After Final communications.
- 22. Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is 703-308-0956.

HP Hoai Pham May 2, 2003

SUPERVISORY PRIMARY EXCENTED
TECHNOLOGY CENTER 2000